

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sunil Talwar et al.

Title: LOGIC CIRCUIT AND METHOD FOR CARRY AND SUM GENERATION AND METHOD OF DESIGNING SUCH A LOGIC CIRCUIT

Docket No.: 1365.063US1

Serial No.: 10/714,408

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Due Date: N/A

Examiner: Unknown

Group Art Unit: 2124

MS Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

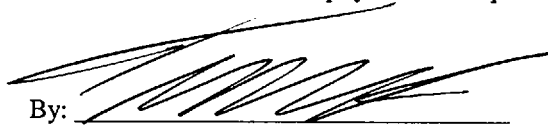
We are transmitting herewith the following attached items (as indicated with an "X"):

X Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.).

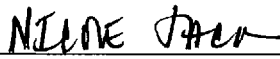
If not provided in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

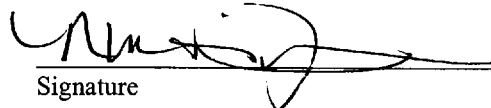
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By: 
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22 day of February, 2007.


Name


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(GENERAL)